AMENDMENTS TO THE CLAIMS

1-78. (Canceled)

79. (New) A display comprising:

{Sig} number of signal lines configured to receive signal potentials;

{Gen} number of general driver circuits, each of the general driver circuits having {G-out} number of output terminals configured to provide said signal potentials to {G-out} number of the signal lines; and

only one fraction driver circuit having {F-out} number of output terminals, said fraction driver circuit being configured to provide said signal potentials to {F-out} number of the signal lines,

wherein $\{Sig\} = (\{Gen\} \times \{G\text{-}out\}) + \{F\text{-}out\}$, with:

{Sig} being the total number of said signal lines that are configured to receive said signal potentials,

{Gen} being an integer value greater than one,

{G-out} being an integer value greater than one, and

{F-out} being an integer value greater than one but less than {G-out}.

80. (New) The display according to claim 79, wherein each of the signal lines in the {G-out} number of the signal lines differ from any of the signal lines in {F-out} number of the signal lines.

81. (New) The display according to claim 79, wherein said general driver circuits and said fraction driver circuit are disposed along a row of driver circuits, said row of driver circuits terminating at said fraction driver circuit.

82. (New) The display according to claim 79, wherein one of the general driver circuits has a general driver horizontal shift register circuit.

83. (New) The display according to claim 82, wherein said fraction driver circuit has a fraction driver circuit horizontal shift register circuit, said fraction driver circuit horizontal shift register circuit being separate and distinct from said general driver horizontal shift register circuit.

84. (New) The display according to claim 82, further comprising:

sampling switches electrically connected between said general driver horizontal shift register circuit and a level shifter;

a data latch circuit electrically connected between said level shifter and a digital-to-analog converter, said digital-to-analog converter being configured to provide said signal potentials to {G-out} number of the signal lines.

85. (New) The display according to claim 79, wherein each of the signal lines has a first time-divided signal line, a second time-divided signal line, and a third time-divided signal line.

86. (New) The display according to claim 85, further comprising:

time-divisional switches configured to selectively provide one of the signal potentials to said first time-divided signal line, said second time-divided signal line, or said third time-divided signal line during a time period.

87. (New) The display according to claim 79, further comprising:

a multiple number of gate lines extending in a gate line direction, each of the signal lines intersecting each of the gate lines.

88. (New) The display according to claim 87, wherein said signal lines extend in a direction other than said gate line direction.

89. (New) The display according to claim 87, wherein a pixel is located at an intersection of one of the gate lines and one of the signal lines.

90. (New) The display according to claim 89, wherein said pixel is on display portion of a transparent insulating substrate, said general driver circuits and said fraction driver circuit not being on said transparent insulating substrate.

91. (New) The display according to claim 87, further comprising:

{Gen} number of general driver circuit connecting portions and {Gen} number of general driver circuit flexible cables,

wherein one of the {Gen} number of general driver circuits connecting portions and one of the {Gen} number of general driver circuit flexible cables are configured to electrically connect one of the {Gen} number of general driver circuits to and one of the {G-out} number of the signal lines.

92. (New) The display according to claim 91, wherein another of the {Gen} number of general driver circuit connecting portions and another of the {Gen} number of general driver circuit flexible cables are configured to electrically connect another of the {Gen} number of general driver circuits to another of the {G-out} number of the signal lines.

93. (New) The display according to claim 91, further comprising:

a fraction driver circuit connecting portion and a fraction driver circuit driver circuit flexible cable,

wherein said fraction driver circuit driver circuit connecting portion and said fraction driver circuit flexible cables are configured to electrically connect said fraction driver circuit to {F-out} number of the signal lines.

94. (New) The display according to claim 79, wherein:

{Gen} = 25;

{G-out} = 120;

{F-out} = 72.

95. (New) The display according to claim 79, wherein said signal potentials on odd numbers of the signal lines are non-inverted, said signal potentials on even numbers of the signal lines being inverted.

96. (New) The display according to claim 79, further comprising:

a memory circuit configured to storing data to be written into said fraction driver circuit driver circuit and said general driver circuits; and

a control circuit configured to simultaneously write different data from said memory circuit to said fraction driver circuit driver circuit and said general driver circuits.

97. (New) The display according to claim 79, wherein said display is a liquid crystal display, a back light being on a back side of a liquid crystal.